Physikalisches Kolloquium

Universität Konstanz

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15:15 Uhr
Zoom-Meeting

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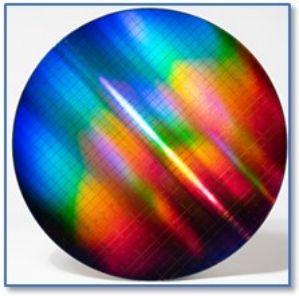
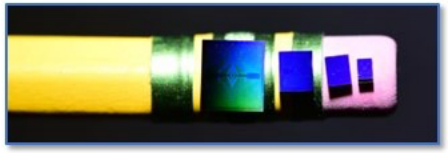
Towards a large scale quantum computer using advanced fabrication technologies





A large scale quantum computer could change the world. Performing certain calculations in minutes that would take the largest supercomputer millions of year. The impact to applications such as cryptography, chemistry, finance, etc would be huge.

Today's quantum processors are limited to 10's of entangled quantum bits. If you believe the hype, a commercially relevant system is just around the corner that can outperform our largest supercomputers. The reality, however, is that we are still at mile 1 of a marathon. There are many unanswered fundamental questions. At Intel, our approach is to rely on the continued evolution of Moore's Law to build qubit arrays with a high degree of process control.

Here, we present progress toward the realization of 300mm Si-MOS based spin qubit devices in a production environment. This includes (i) isotopically purified ^{28}Si epi substrates with a compelling substrate quality (ii) design of a custom qubit layout, (iii) integration of fin-based spin qubit devices using immersion lithography, moving from classical transistor structures to full spin qubits, and (iv) the realization of quantum dots in a nested gate design novel to a 300mm process line.

In addition, this talk will focus on two bottlenecks to moving beyond today's few-qubit devices. The first bottleneck is in the interconnect design of the quantum circuit. Today's qubits have personalities. Individual control of each qubit is required. A small quantum processor today has multiple RF and DC wires per qubit. This is a brute force approach to wiring and will not scale to the millions of qubits needed for large applications.

The second bottleneck relates to the speed of information turns in quantum development. Fabrication of spin qubits in a silicon substrate bares similarity to conventional transistors from advanced CMOS technologies. One of the above 300mm wafers has over 10,000 individual quantum test structures. Naturally, R&D should be accelerated by the potential volume of statistical data. While automated electrical testing of a CMOS transistor wafer can be completed in less than an hour at room temperature, data collection at cryogenic temperatures is currently limited to a small number of devices with a turnaround of hours to days. Rhetorically speaking, "How can we deliver an exponentially fast compute technology with slow and serial characterization of quantum chips?"